IN THE CLAIMS:

Please amend the claims as set forth below.

1. (Currently Amended) A decode unit coupled to receive instruction bytes, the decode unit coupled to dispatch instructions to an execution subsystem, wherein the decode unit comprises circuitry divided into a pipeline including a plurality of pipeline stages, the circuitry configured to concurrently initiate decode of a plurality of instructions having a program order with respect to each other, wherein the circuitry is configured to dispatch at least an initial instruction of the plurality of instructions from a first pipeline stage of the plurality of pipeline stages, and wherein the circuitry is configured to dispatch at least one remaining instruction of the plurality of instructions from a second pipeline stage of the plurality of pipeline stages, and wherein the second pipeline stage is subsequent to the first pipeline stage in the pipeline.

2. (Original) The decode unit as recited in claim 1 wherein the circuitry is configured to dispatch each remaining instruction of the plurality of instructions from the second pipeline stage.

3. (Original) The decode unit as recited in claim 2 wherein the second pipeline stage is a last stage of the pipeline.

4. (Currently Amended) ~~The decode unit as recited in claim 1~~ A decode unit coupled to receive instruction bytes, the decode unit coupled to dispatch instructions to an execution subsystem, wherein the decode unit comprises circuitry divided into a pipeline including a plurality of pipeline stages, the circuitry configured to concurrently initiate decode of a plurality of instructions, wherein the circuitry is configured to dispatch at least an initial instruction of the plurality of instructions from a first pipeline stage of the plurality of pipeline stages, and wherein the circuitry is configured to dispatch at least one remaining instruction of the plurality of instructions from a second pipeline stage of the plurality of pipeline stages, and wherein the second pipeline stage is subsequent to the first pipeline stage in the pipeline, and wherein the decode unit is configured to dispatch instructions

into a plurality of positions input to the execution subsystem, wherein the plurality of positions are indicative of a program order of the instructions concurrently dispatched into the plurality of positions.

5. (Original) The decode unit as recited in claim 4 wherein the circuitry is configured to dispatch the initial instruction into a last position of the plurality of positions, the last position being ordered subsequent to each other one of the plurality of positions.

6. (Original) The decode unit as recited in claim 5 wherein the circuitry is configured to dispatch the remaining instructions into other ones of the plurality of positions.

7. (Original) The decode unit as recited in claim 6 wherein the decode unit is coupled to receive a second plurality of instructions subsequent to the plurality of instructions, and wherein the circuitry is configured to dispatch at least a second initial instruction of the second plurality of instructions into one or more of the last positions concurrent with dispatching the remaining instructions.

8. (Original) The decode unit as recited in claim 4 wherein the circuitry is configured to dispatch a plurality of initial instructions from the first pipeline stage into a plurality of last positions of the plurality of positions.

9. (Original) The decode unit as recited in claim 1 wherein the plurality of instructions are variable length.

10. (Original) The decode unit as recited in claim 1 wherein the circuitry includes a first circuit operable on the initial instruction in a third stage of the plurality of pipeline stages, the first circuit configured to perform a first portion of decoding the initial instruction, and wherein the circuitry further includes a second circuit operable on the remaining instruction in a fourth pipeline stage of the plurality of pipeline stages, the fourth circuit configured to perform the first portion of decoding the remaining instruction.

11. (Currently Amended) A processor comprising:

a decode unit coupled to receive instruction bytes, wherein the decode unit comprises circuitry divided into a pipeline including a plurality of pipeline stages, the circuitry configured to concurrently initiate decode of a plurality of instructions having a program order with respect to each other, wherein the circuitry is configured to dispatch at least an initial instruction of the plurality of instructions from a first pipeline stage of the plurality of pipeline stages, and wherein the circuitry is configured to dispatch at least one remaining instruction of the plurality of instructions from a second pipeline stage of the plurality of pipeline stages, and wherein the second pipeline stage is subsequent to the first pipeline stage in the pipeline; and

an execution subsystem coupled to receive the initial instruction and the remaining instruction and configured to execute the initial instruction and the remaining instruction.

12. (Original) The processor as recited in claim 11 wherein the circuitry is configured to dispatch each remaining instruction of the plurality of instructions from the second pipeline stage.

13. (Original) The processor as recited in claim 12 wherein the second pipeline stage is a last stage of the pipeline.

14. (Currently Amended) ~~The processor as recited in claim 11~~ A processor comprising:

a decode unit coupled to receive instruction bytes, wherein the decode unit comprises circuitry divided into a pipeline including a plurality of pipeline stages, the circuitry configured to concurrently initiate decode of a plurality of instructions, wherein the circuitry is configured to dispatch at least an initial instruction of the plurality of instructions from a first

pipeline stage of the plurality of pipeline stages, and wherein the circuitry is configured to dispatch at least one remaining instruction of the plurality of instructions from a second pipeline stage of the plurality of pipeline stages, and wherein the second pipeline stage is subsequent to the first pipeline stage in the pipeline; and

an execution subsystem coupled to receive the initial instruction and the remaining instruction and configured to execute the initial instruction and the remaining instruction, and wherein the decode unit is configured to dispatch instructions into a plurality of positions input to the execution subsystem, wherein the plurality of positions are indicative, to the execution subsystem, of a program order of the instructions concurrently dispatched into the plurality of positions.

15. (Original) The processor as recited in claim 14 wherein the circuitry is configured to dispatch the initial instruction into a last position of the plurality of positions, the last position being ordered subsequent to each other one of the plurality of positions.

16. (Original) The processor as recited in claim 15 wherein the circuitry is configured to dispatch the remaining instructions into other ones of the plurality of positions.

17. (Original) The processor as recited in claim 16 wherein the decode unit is coupled to receive a second plurality of instructions subsequent to the plurality of instructions, and wherein the circuitry is configured to dispatch at least a second initial instruction of the second plurality of instructions into one or more of the last positions concurrent with dispatching the remaining instructions.

18. (Currently Amended) The processor as recited in claim ~~11~~ 14 wherein the decode unit is configured to dispatch a plurality of initial instructions from the first pipeline stage into a plurality of last positions of the plurality of positions.

19. (Original) The processor as recited in claim 11 wherein the plurality of instructions are variable length.

20. (Original) The processor as recited in claim 11 wherein the circuitry includes a first circuit operable on the initial instruction in a third stage of the plurality of pipeline stages, the first circuit configured to perform a first portion of decoding the initial instruction, and wherein the circuitry further includes a second circuit operable on the remaining instruction in a fourth pipeline stage of the plurality of pipeline stages, the fourth circuit configured to perform the first portion of decoding the remaining instruction.

21. (Original) A decode unit coupled to receive instruction bytes, the decode unit coupled to dispatch instructions into a plurality of positions input to an execution subsystem, wherein the plurality of positions are indicative, to the execution subsystem, of a program order of instructions concurrently dispatched into the plurality of positions, wherein the decode unit is configured to concurrently initiate decode of a plurality of instructions, and wherein the decode unit is configured to decode one or more initial instructions of the plurality of instructions with a first decode latency and to dispatch the one or more initial instructions into one or more last positions of the plurality of positions, the last positions being ordered subsequent to each of the other positions of the plurality of positions, and wherein the decode unit is configured to decode at least one remaining instruction with a second decode latency and to dispatch the remaining instruction into a different one of the plurality of positions.

22. (Original) The decode unit as recited in claim 21 wherein the decode unit is coupled to concurrently receive a second plurality of instructions, and wherein the decode unit is configured to decode a second one or more initial instructions of the second plurality of instructions and to dispatch the second initial instructions into the one or more last position concurrently with dispatching the remaining instruction into the different one of the plurality of positions.

23. (New) A computer system comprising:

a processor comprising:

a decode unit coupled to receive instruction bytes, wherein the decode unit comprises circuitry divided into a pipeline including a plurality of pipeline stages, the circuitry configured to concurrently initiate decode of a plurality of instructions having a program order with respect to each other, wherein the circuitry is configured to dispatch at least an initial instruction of the plurality of instructions from a first pipeline stage of the plurality of pipeline stages, and wherein the circuitry is configured to dispatch at least one remaining instruction of the plurality of instructions from a second pipeline stage of the plurality of pipeline stages, and wherein the second pipeline stage is subsequent to the first pipeline stage in the pipeline; and

an execution subsystem coupled to receive the initial instruction and the remaining instruction and configured to execute the initial instruction and the remaining instruction; and

a peripheral device configured to communicate between the computer system and another computer system.

24. (New) The computer system as recited in claim 23 wherein the peripheral device comprises a modem.

25. (New) The computer system as recited in claim 23 wherein the peripheral device comprises a network card.

26. (New) The computer system as recited in claim 23 further comprising an audio device.

27. (New) A method comprising:

in a decode unit, concurrently initiating decode of a plurality of instructions having a program order with respect to each other, wherein the decode unit includes a pipeline divided into a plurality of pipeline stages;

the decode unit dispatching at least an initial instruction of the plurality of instructions from a first pipeline stage of the plurality of pipeline stages; and

the decode unit dispatching at least one remaining instruction of the plurality of instructions from a second pipeline stage of the plurality of pipeline stages, and wherein the second pipeline stage is subsequent to the first pipeline stage in the pipeline.

28. (New) The method as recited in claim 27 wherein the dispatching is into a plurality of positions input to the execution subsystem, wherein the plurality of positions are indicative of a program order of the instructions concurrently dispatched into the plurality of positions.

29. (New) The method as recited in claim 28 wherein dispatching the initial instruction comprises dispatching into a last position of the plurality of positions, the last position being ordered subsequent to each other one of the plurality of positions.

30. (New) The method as recited in claim 29 wherein dispatch the remaining instruction comprises dispatching into another one of the plurality of positions.

31. (New) The method as recited in claim 30 further comprising

the decode unit receiving a second plurality of instructions subsequent to the

plurality of instructions; and

the decode unit dispatching at least a second initial instruction of the second plurality of instructions into one or more of the last positions concurrent with dispatching the remaining instruction.